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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,587	02/21/2001	Dug Jin Park	8733.389.00	8760

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EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,587	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U S C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7,9,11,12 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,9,11,12 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-7, 9, 11-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (AAPA) in view of US 6,022,753 (Park et al) and US 6,077,643 (kumar et al).

Claims 5,14 and 9, 11, 12, AAPA discloses (page 2, line 11 – page 5, line 6; Figs.1A – 1E) that a method of fabricating a liquid crystal display device having a thin film transistor with a gate electrode (13), a gate insulating film (15), an active layer (17), an ohmic contact layer (19), and source electrode (21), drain electrode (22) on a transparent substrate (11) (or forming a thin film transistor having a gate electrode 13, a source electrode 21, and a drain electrode 22 on a transparent substrate 11), and the gate line connected to the gate electrode, the data line (23) connected to the source electrode (21) that define a pixel area; and the method comprising the steps of:

- forming a passivation layer (25) covering the thin film transistor, the gate line and the date line on the transparent substrate (11); and patterning the passivation layer (25) to define a contact hole (26) for exposing the drain electrode (22);

- forming a transparent conductive film (27) being in contact with the drain electrode (22) via the contact hole (26) on the passivation layer (25);
- the exposing step is the ultraviolet ray selectively irradiated onto the photoresist (29) using an exposure mask (31) having a shielding part (32) (opaque part) and a transparent part (33) (page 4, lines 14-20; Figs.1D-1E), i.e., using an exposure mask to expose the photoresist by the light passing through the transparent part of the exposure mask.

AAPA does not expressly disclose that coating a negative-type photoresist on the transparent conductive film and then exposing the negative-type photoresist with an image of pixel electrode, other than a portion corresponding to data line, gate line and TFT area; and developing the photoresist such that the unexposed area is removed; patterning the transparent conductive film using the photoresist pattern as a mask to form a pixel electrode in contact with the drain electrode via the contact hole; and soft-baked the coating and post exposure baking; and then removing the photoresist pattern.

However, Park discloses (col.4, line 22 – col. 5, line 30; Figs. 5A – 5D and 6A – 6D) that a manufacturing method of forming a pixel electrode by using a negative photoresist and by a front exposure in which the photoresist (1000) is formed on the transparent conductive layer (ITO) (800), so that the negative photoresist remains when exposed by light, such that the light is irradiated from the front side of the substrate (100) is executed by using a mask having opening pattern over portions of the negative photoresist (1000) on the pixel region (P), and then the exposed portions remains after

development, and the ITO layer (800) is etched by using the remaining photoresist as an etch mask to form a pixel electrode (810).

Park also discloses (col.5, lines 31-34) that in the manufacturing method, the pixel electrode (810) overlaps the gate line (200), the gate electrode (210) and data line (600), but the pixel electrode (810) may not overlap them. Therefore, forming an exposed area defining a pixel area also can be other than a portion corresponding to the data line, the gate line and the thin film transistor area, because the fundamental principle is the same as using negative photoresist coating and exposing to light would remove the unexposed portions.

Park indicates (col.5, lines 16-30) that forming the pixel electrode (810) by using the negative photoresist, the pixel defects decreased compared with using a positive photoresist through the front exposure, because if there exist some particles on the unexposed portions of the negative photoresist to light which would cause the adjacent pixel electrodes electrically shorted would be removed (the unexposed portions of the negative photoresist to light is removed).

Kumar discloses (col.12, lines 65 – 68) that the photoresist composition is softbaked at 120 °C. And the photoresist is a kind of actinic resin, so that coating the photoresist must have a certain thickness and in order to make adhesive the coating that must be hardening and first must be softbaked at a certain temperature, and those skilled in the art would find a proper thickness, such as 1 – 2 μm and a proper softbaking temperature such as 100 – 125°C, and that would have been at least obvious. Kumar also discloses (col.12, line 67 – col.13, line 14) that the resist coating

layer after exposure to the light would be post-exposure baked (PEB) at temperature range110 - 140°C to obtain a certain dissolution rate.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to coat a negative-type photoresist on the transparent conductive film and forming an exposed area defining a pixel area, then exposing the negative-type photoresist with an image of a pixel electrode, then developing the photoresist in which the unexposed area is removed, then patterning the transparent conductive film using the photoresist as a mask to form a pixel electrode in contact with the drain electrode via the contact hole, then remove the photoresist pattern as claimed in claims 5,14, 9, 11 and 12. Since coating a negative-type photoresist and exposing by light and then soft-baking, post baking would harden the coating and obtaining a certain dissolution rate, and that would decrease the adjacent pixel electrodes electrically shorted defects.

Claim 6, Park discloses (col.5, lines 1-15; Fig.6) that the light exposure is executed by using a mask (exposure mask) having opening pattern (the exposure part) over the portions of the negative photoresist (1000) on the pixel region (P) (Fig.6A) (corresponding to the pixel area), so that the shielding part of the exposure mask would corresponding to the data line, gate line and the thin film transistor area (Fig.6A), such that the unexposed portions of the negative photoresist to light would be removed, so as to prevent the adjacent pixel shorting defects.

Therefore, it would have been obvious to those skilled in the art to use the exposure mask as claimed in claim 6 for removing the unexposed portions of the negative photoresist, so as to prevent the adjacent pixel shorting defects.

Claims 7 and 16, AAPA (page 4, lines 21 – 22; Fig.1D-1E) that the photoresist (29) is developed with a developer, such as aqueous alkali solution, and those skilled in the art would find a proper time to obtain a proper developing the photoresist such as 60 – 120 seconds, and that would have been at least obvious.

Claim 15, AAPA discloses (page 5, lines 1-6; Figs.1D-1E) that patterning the transparent conductive film (27) uses a mixed acid as an etchant liquid, and that is using a wet etchant.

Claims 17-18, AAPA discloses (page 4, lines 9-13; Figs.1D-1E) that the passivation layer (25) is patterned to define a control hole (26) so as to expose the drain electrode (22), and the transparent conductive material (ITO) is deposited on the passivation layer (25) so as to electrically contact the drain electrode (22) via the contact hole (26).

Response to Arguments

3. Applicant's arguments filed on Mar.7, 2003 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) None of the references teach the features of the claims, such as coating the transparent conductive with a negative-type photoresist into 1.0 to 2.0 μm, and using soft-bakeing at 100 to 150 °C and post baking at 125 to 145 °C.

Examiner's responses to Applicant's **only** arguments are as follows:

1) Park discloses (col.4, line 22 – col. 5, line 30; Figs. 5A – 5D and 6A – 6D) that a manufacturing method of forming a pixel electrode by using a negative photoresist and by a front exposure in which the photoresist (1000) is formed on the transparent conductive layer (ITO) (800), so that the negative photoresist remains when exposed by light, such that the light is irradiated from the front side of the substrate (100) is executed by using a mask having opening pattern over portions of the negative photoresist (1000) on the pixel region (P), and then the exposed portions remains after development, and the ITO layer (800) is etched by using the remaining photoresist as an etch mask to form a pixel electrode (810).

Kumar discloses (col.12, lines 65 – 68) that the photoresist composition is softbaked at 120 °C. And the photoresist is a kind of actinic resin, so that coating the photoresist must have a certain thickness and in order to make adhesive the coating that must be hardening and first must be softbaked at a certain temperature, and those skilled in the art would find a proper thickness, such as 1 – 2 μm and a proper softbaking temperature such as 100 – 125°C, and that would have been at least obvious. Kumar also discloses (col.12, line 67 – col.13, line 14) that the resist coating layer after exposure to the light would be post-exposure baked (PEB) at temperature range110 - 140°C to obtain a certain dissolution rate.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213. The examiner can normally be reached on 349.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
June 6, 2003